Claim 29: (New)

A semiconductor memory in a chip, comprising:

a plurality of memory cells, each cell having at least a transfer MOS transistor;

a plurality of word lines, each word line coupled with gate electrodes of said transfer MOS transistors of said plurality of memory cells;

a plurality of data lines, each data line coupled with drain electrodes of said transfer MOS transistors of said plurality of memory cells;

a word driver circuit that provides an output voltage to of said plurality of word lines; and

a voltage generator circuit that includes a charge pump circuit receiving a periodic signal and an operating voltage to generate a first voltage, and provides said first voltage to said word driver circuit,

wherein the amplitude of said first voltage is larger than that of a voltage associated with said data lines;

wherein said word driver circuit provides said first voltage to said word line to activate said one word line.

Claim 30: (New)

The semiconductor memory according to claim 29, wherein said voltage generator circuit includes a detector circuit also which provides a signal to make said charge pump circuit stop receiving said periodic signal when a voltage level of said periodic signal is larger than predetermined voltage.

Claim 31: (New)

The semiconductor memory according to claim 30, wherein said word driver circuit includes a p-channel MOS transistor whose source receives said first voltage and whose drain provides a voltage to activate said word line when said word driver circuit is activated.

Claim 32: (New)

The semiconductor memory according to claim 29, wherein said voltage generator circuit includes a voltage clamp circuit to thereby clamp said first voltage to predetermined voltage.

Claim 33: (New)

The semiconductor memory according to claim 29, wherein said semiconductor memory is a dynamic random access memory.

REMARKS

Claims 21 to 33 are now in this application. New claims 29 to 33 have been added.

The Examiner has rejected claims 21-28 under the doctrine of obvious-type double patenting, stating that the claims are unpatentable over claims 1-7 of U.S. Patent No. 5,377,156. As suggested by the Examiner, the attached Terminal Disclaimer has been executed to overcome this rejection. The Disclaimer has been executed by the undersigned who is an attorney of record in this case and who has been an associate power of attorney by his partner Edward W. Greason.